On Channel Shape Variation of 10-nm-Gate Gate-All-Around Silicon Nanowire MOSFETs

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Abstract

Recently, gate-all-around (GAA) nanowire field effect transistors (NWFETs) have attracted increasing attention due to their superior gate control and short channel effect immunity [1-4]. However, confined by the limitation of manufacturing process, the different aspect ratio (AR) results in different shapes of channel cross section, such as ellipse-shaped or rectangular-shaped instead of the ideal round-shaped and square-shaped, respectively [5-8].

In this study, we analyze the effects on 10-nm-gate single- and multi-channel GAA silicon NWFETs with different geometry of cross-section, including AR and radius variation by applying an experimentally validated three-dimension (3D) quantum correction simulation. We point out that an ellipse-shaped GAA NWFETs having relatively smaller AR of radius owns better electrical characteristics. As the technology nodes have channel length in nanoscale regime, therefore, it becomes necessary to include quantum mechanical effects when modeling any FET's terminal property. To model the quantum mechanical effects, we adopt a computationally cost-effective simulation model which consists of drift-diffusion equations with doping-/field-dependent, channel orientation dependent, and surface roughness mobility for the carrier's transport and density-gradient equations for various quantum mechanical effects [9]. The computational architecture of the 3D single-channel NWFET and cross-section views of channel are shown in Fig. 1(a). Figure 1(b) shows the achieved electrical characteristics of single-channel GAA NWFETs. In the case of AR = 0.5, the value of its subthredshold swing (SS) and drain induced barrier lowering (DIBL) is 66 $mVdec^{-1}$ and 68 mVV^{-1}, respectively, and the order of magnitude of I_{on}/I_{off} ratio reaches 6. However, for the case of AR = 2, has SS and DIBL are considerably larger at 116 $mVdec^{-1}$ and 113 mVV^{-1}, respectively and the I_{on}/I_{off} ratio is in the order of 4. It is obvious that when the AR decreases, the device shows better channel controllability. In addition, the device with a smaller AR demonstrates better operating characteristics and suffers from less short-channel effects.

Figure 2 illustrates a transformation between ellipse to circle shaped cross-section of effective radius R_{eff} and corresponding I_D-V_G characteristics. As can be seen, the device with the smallest R_{eff} has the best I_{on}/I_{off} ratio of all, but the case of the largest R_{eff} (i.e. AR = 2) has the worst. This improvement is attributed to the effective gate control due to relatively smaller radius of the cross-section. For multi-channel cases, we focus on the two-channel devices. Figure 3(a) is the 3D two-channel NWFET structure and its corresponding cross-section views respectively. The case of two-channel with AR equal to 0.5 has the best short-channel effect parameters (i.e. I_{on}/I_{off} ratio, SS, and DIBL), which is shown in Fig. 3(b) among all the six cases. It also improves upon the values as compared with the single-channel case with AR = 0.5, while opposite is true for dual channels with AR = 2. Furthermore, it can be seen that two-channel case with both AR equal to 2 has the worst properties. The order of the I_{on}/I_{off} ratio of it has degenerated to 3, and the DIBL is even worse. Consequently, the ability of suppressing short-channel effect of the structure with smaller AR is much better than that with the larger one. In summary, electrical characteristic of 10-nm-Gate silicon NWFET with various process variation of channel radius has been studied. We are currently studying NWFET with different channel materials.

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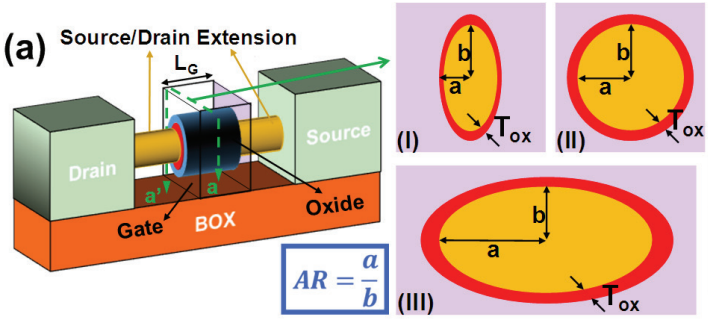
Figures



(b)

Single-channel devices	I_{on}/I_{off} ratio	SS (mV/dec)	DIBL (mV/V)
AR 0.5	1.866e6	66	68
AR 1	1.015e5	87	99
AR 2	1.204e4	116	113

Figure 1. (a) Three-dimensional plot of single-channel GAA nanowire transistor structure and the cross-sectional views with different AR equal to (I) 0.5, (II) 1, and (III) 2, respectively. The testing device has gate length L_G= 10nm and oxide thickness T_{ox}= 0.8nm. (b) Electrical characteristic of the device for different AR.

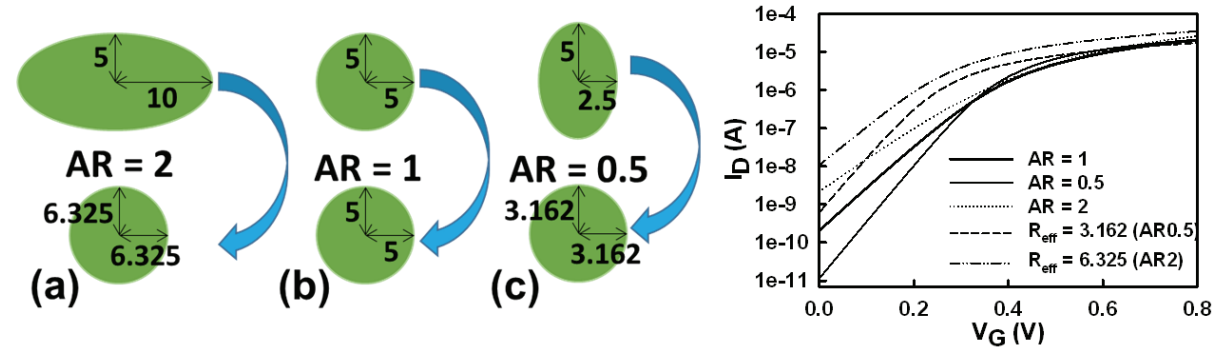
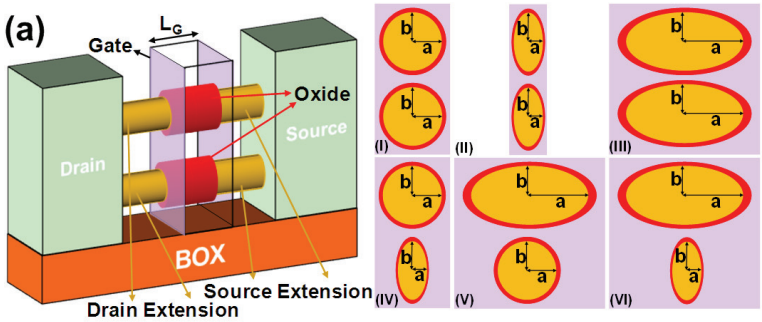


Figure 2. (a)-(c) The elliptical cross-section transformations to a circular shape of effective radius R_{eff}. The right plot shows the I_D-V_G curves of the single channel NWFET for different AR and effective radius.



(b)

Two-channel devices	I_{on}/I_{off} ratio	SS (mV/dec)	DIBL (mV/V)
AR 0.5&0.5	4.127e6	63	17
AR 1&1	1.757e5	69	72
AR 2&2	1.694e3	79	312
AR 1&0.5	1.405e5	69	65
AR 1&2	1.283e4	76	141
AR 0.5&2	1.18e4	77	128

Figure 3. (a) Multi-channel Si NWFET with different AR equal to (I) 1 and 1, (II) 0.5 and 0.5, (III) 2 and 2, (IV) 1 and 0.5, (V) 1 and 2, and (VI) 0.5 and 2, respectively. (b) Electrical characteristic of the device for different AR.